

## Abstract:

With recent improvements in silicon fabrication technology, reconfigurable devices can now be applied to accelerate functions beyond the traditional computing domains. In-network processing and smart computational storage are just two of these approaches. We discuss both simple and more complex application examples for both of these domains, covering a network-attached ML inference appliance, a JOIN accelerator for distributed databases, and also look forward to using a cache-coherent interconnect, such as CCIX or CXL, to tackle a complex database acceleration scenario linking a computational storage unit using near-data processing to a full-scale PostgreSQL database system. Beyond these hardware architectures, the talk also examines improvements in programming tools specialized for the realization of reconfigurable computing systems. Using the open-source TaPaSCo framework as an example, advanced features such as on-chip dynamic parallelism, flexibly customizable inter-processing element communications, and host/accelerator shared virtual memory with physical page migration capabilities are discussed.

## **Biography:**

Prof. Andreas KOCH is a full professor at TU Darmstadt in Germany, where he leads the Embedded Systems and Applications Group. He has been working on accelerated computing since the early 1990s, mainly using reconfigurable devices such as FPGAs and CGRAs, but also considering GPUs and specialized ML accelerators. He has always "played on both sides of the fence", performing research not only on hardware architectures, but also on the software tools and libraries required to exploit them. Among others, he is currently applying his expertise to the domains of storage acceleration, near-data and in-network processing as well as ML inference for sum-product networks.

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