

CityU Architecture Lab for Arithmetic and Security (CALAS) Seminar Series

FPGA Architecture and Tool Research with Cross-Layer Optimization

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Abstract:

Field Programmable Gate Array (FPGA) combines the programmability of a processor with the relatively high performance of an application-specific integrated circuit. It is an important energy-efficient computing platform. In the research of FPGA, we noticed that on the one hand, the architecture and design automation tools of FPGA have a high degree of interaction with each other. On the other hand, they face the challenges and opportunities of semiconductor underlying process devices and the application of new upper-layer algorithms. This talk will introduce our cross-layer optimization of FPGA architecture and tool research from several aspects such as energy-efficient FPGA, process deviation-sensitive FPGA, scalable FPGA, and new FPGA applications.

Biography:

Yajun HA received the B.S. degree from Zhejiang University, Hangzhou, China, in 1996, the M.Eng. degree from the National University of Singapore, Singapore, in 1999, and the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 2004, all in electrical engineering. He is currently a Professor at ShanghaiTech University, China. He has been awarded several important Natural Science and Foundation China (NSFC) funding, including "The Research Fund for International Senior Scientist" and "Major International (Regional) Joint Research Project". He served as the Editor-in-Chief for the IEEE Trans. on Circuits and Systems II: Express Briefs (2022–2023). Before joining ShanghaiTech University, he was a Director of the I2R-BYD Joint Lab at Institute for Infocomm Research, Singapore, and an Adjunct Associate Professor at the Department of Electrical & Computer Engineering, National University of Singapore. Prior to this, he was an Assistant Professor with National University of Singapore. His research interests are focused on energy efficient circuits and systems, including reconfigurable computing, ultra-low power digital circuits and systems, embedded system architecture and design tools for applications in robots, smart vehicles and intelligent systems. He has published more than 150 internationally peer-reviewed journal/conference papers on these topics. He is the recipient of several IEEE/ACM Best Paper Awards.