Department of Electrical Engineering
香港城市大學
City University of Hong Kong

CityU Architecture Lab for Arithmetic and Security (CALAS) Seminar Series

Low-Level Security and Assurance in FPGA Systems

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Abstract:

Field-Programmable Gate Arrays (FPGAs) are increasingly deployed in mission-critical domains such as defense, biomedical systems, secure communications, and autonomous vehicles. In these settings, ensuring the integrity and trustworthiness of FPGA-based systems is essential—from the hardware compilation process to deployment in the field. This talk presents a series of research projects addressing key challenges in FPGA security: (1) securing the FPGA compilation and CAD flow against tampering and leakage, (2) protecting intellectual property at the bitstream level, (3) evaluating and mitigating attacks on device authentication mechanisms such as PUFs, and (4) investigating reverse engineering techniques to understand and defend against IP extraction. A common thread across these efforts is the importance of understanding how high-level designs map to bitstream-level implementations, in order to support more effective security and analysis.

Biography:

Dr. Jeff Goeders is an Associate Professor and the graduate coordinator in the Department of Electrical and Computer Engineering at Brigham Young University (BYU) in Provo, Utah. He received his BASc in Computer Engineering from the University of Toronto in 2010, and MASc and PhD degrees from the University of British Columbia in 2012 and 2016, respectively. His research focuses on reconfigurable computing and embedded systems, with an emphasis on FPGA security, debugging technologies, open-source hardware compilers, and system reliability. He is a Senior Member of both IEEE and ACM.

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